IC693CPU350

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May 16, 2008
GFK-1512R

IMPORTANT PRODUCT INFORMATION

READ THIS INFORMATION FIRST

Product: Series 90-30 CPU Modules with Firmware Release 10.74

IC693CPU350-EJ
IC693CPU360-EK
IC693CPU363-DK

This hardware revision replaces an obsolete cache RAM with a component that is currently available. At room temperature, the new part reduces the battery life from 6 years to 10 months.

Firmware version 10.74 is a maintenance release that consists of the changes described in "Problems Resolved by this Firmware Revision" on page 2.

Upgrades

No field upgrade is required or available for this hardware revision.

If you wish to upgrade an existing CPU350, CPU360 or CPU363 to firmware version 10.74, you may purchase the applicable kit or download it at no charge from http://support.gefanuc.com/. Firmware upgrades require the IC690ACC901 Miniconverter and Cable Kit.

CPU Part Numbers for Firmware Version 10.74	Firmware Upgrade Kit Part Number
IC693CPU350-xJ	44A747145-G08
IC693CPU360-xK	44A747148-G09
IC693CPU363-xK	44A747766-G09

Functional Compatibility

- With the original cache RAM component, the battery life was 6 years 25°C and 1½ years at 60°C. The data retention current on the currently available part reduces the battery life to 10 months at 25°C and 5½ months at 60°C.
- Machine Edition PLC Logic Developer version 2.11 or later, or VersaPro version 2.02 or later should be used to configure and program these CPU models.
- Version 4.00 or later of the C toolkit must be used for C programming.
- All Ethernet Interface (IC693CMM321) modules used for programmer or HMI/SCADA communications with this CPU must be one of the following revision groups:

  IC693CMM321-CC or later

  IC693CMM321-AA or -BA upgraded to firmware version 1.11 or later
- The CPU363 model does not support configuration of communications (other than SNP Slave through the power supply port) using the Hand-Held Programmer (HHP).
- IC693BEM340 FIP Bus Controller firmware version 3.00 or later is required for this release of CPU firmware.

Problems Resolved by this Hardware Revision

The original cache RAM component is obsolete and no longer available. The new component is the lowest power part currently available.

Problems Resolved by this Firmware Revision

Loss/add of module faults with IC693ALG222/223 modules in CPU350, CPU360 or CPU363 PLC

In all previous CPU firmware versions, when two or more high-density analog input modules (IC693ALG222 or IC693ALG223) are installed in the CPU rack, and all 16 input channels are active in the modules, loss of module and addition of module faults for one of the analog modules may occur when the CPU rack is powered on. This issue is corrected in version 10.74.

Restrictions and Open Issues

Subject	*Description*
Timing Issue with IC693ALG220/221-F or earlier modules may result in incorrect %AI values read by CPU	The %AI values reported by an IC693ALG220/221-F or earlier module revision may be incorrect and exhibit erratic behavior. Certain current or voltage levels within the input range applied to the module can cause the %AI values to be reported incorrectly. The problem stems from the use of particular opto-couplers that may exhibit timing issues with CPU 35x/36x modules. This issue does not occur with IC693ALG220/221-G and later module revisions.
The CPU may generate a fatal fault if logic containing a DOIO function block call to a smart module is repeatedly transitioned between RUN and STOP modes.	Storing program logic that contains a call to a DOIO function block may cause the CPU to run out of system memory. This can occur when the PLC transitions between RUN and STOP modes several times. Storing the hardware configuration will cause the system memory to be freed, and the PLC will resume normal operation.
CPU may generate a Fatal Fault during store of folders with large configurations	The CPU may generate a fatal fault during a store of a folder with a very large configuration. This may be made worse by storing logic and configuration at the same time, or by read requests for reference table data from a programmer or HMI during the store. See “Storing Large Configurations” on page 3 for recommendations.
Reading corrupted data from flash memory may cause a Watch Dog Timeout	If corrupted data is read from flash memory, the Watch Dog Timer on the PLC may be triggered. This can be corrected by completing a valid flash store.
The CPU may generate a fatal fault when configuring a module with the HHP following a store to the PLC that exhausts user memory	The 90-30 PLC CPU may generate a fatal fault when the user attempts to configure a module with the HHP after a store to the PLC that exhausts user memory.
Firmware Update Fail Following Power-up with Clear M/T and a Write to Flash	A firmware upgrade may fail after the user presses the **Clear** and **M/T** keys on the HHP during power-up and then performs a write to flash. Cycling power on the PLC will enable the upgrade to proceed.

Subject	*Description*
CPU363 ports 1 and 2 do not handle parity errors in accordance with the SNP specification.	The SNP specification requires both slave and master devices to reply to messages that contain parity errors with a 2-byte NACK message indicating a BCC or Parity Error (code 0). The NACK triggers a re-try transmission from the communications partner. For CPU363 ports 1 and 2 however, parity errors are fatal. The ports do not send the NACK message as expected, and the SNP master must send a new Attach message to re-establish communications. During the time between the parity error and the new Attach message, CPU363 ports 1 and 2 do not respond to COMMREQs from the PLC application. For example, attempting to use a serial port setup COMMREQ to change the parity setting will fail if the first Attach message with parity that is different from the hardware configuration arrives at the port before the COMMREQ. If the master re-tries Attach messages more often than every 12 seconds, the COMMREQ will not be processed until the master stops sending Attach messages or the SNP cable is disconnected.

Operating Notes

Subject	*Description*
User Information Cleared when Upgrading Firmware	User information, consisting of program, configuration, CPU ID (used for SNP communications), and status tables in RAM memory, will automatically be cleared if the CPU firmware in flash memory is changed. You will need to restore these if upgrading firmware. The user program, configuration, and reference memory (%R, %AI, %AQ, %I, %Q, %T and %M) tables can be restored from a PLC programmer folder or from flash. The SNP ID must be set separately, using the PLC programmer or the HHP. The faults, overrides and transition tables cannot be stored to flash. The overrides may be restored from the programmer or folder, but the faults and transitions are lost.
Writing to Flash Memory	When writing very large programs to flash memory, it may be necessary to increase the request timeout value in the programming software to avoid receiving a request timeout message. An upper bound of 25 seconds is typically satisfactory
Storing Large Configurations	A Series 90-30 PLC using a CPU 36x supports a maximum of 32 DSM314 or DSM324 modules. This number is reduced when other intelligent modules are used in the PLC, such as APM and GBC modules. It may also be reduced when: The number of racks in the PLC increases; The total size of logic, motion and AUP files increases; The application uses C logic blocks or a C logic program; or Connected programmers or HMI devices are used to read reference memory or fault tables. In some cases it may be possible to increase the number of DSM314 or DSM324 modules that the CPU will accept in the hardware configuration by storing logic first and then storing the configuration separately.
CPU350 and CPU36x do not support hardware configurations for CPU31x/32x/33x/34x/374	An application that contains any CPU35x or CPU36x model in the hardware configuration can usually be stored to any other release 9.00 or later CPU35x or CPU36x model and then executed. However, attempting to store a hardware configuration that contains a CPU31x, 32x, 33x, 34x or 374 to a CPU35x or CPU36x will fail.
Simultaneous Load and Store	When operating with multiple programmers attached, if a store operation is initiated by one programmer, while a load operation is already in progress, the load request will fail.
Transition Tables are not cleared when the reference tables are cleared.	The transition tables are not cleared upon clearing the reference tables through the programmer.

Product Documentation

Series 90-30 PLC Installation and Hardware Manual, GFK-0356
Series 90-30 CPU Reference Manual, GFK-0467
TCP/IP Ethernet Communications for the Series 90 PLC User's Manual, GFK-1541
TCP/IP Ethernet Communications for the Series 90 PLC Station Manager Manual, GFK-1186

Documentation Errata

Battery Life

The new cache RAM component reduces the battery life as shown in the following table. This information will be included in the next scheduled update of the *Series 90-30 CPU Reference Manual.*

Hardware Version	Estimated Battery Life	
	at 25°C	at 60°C
IC693CPU350-Dx , C693CPU360-Dx, IC693CPU363-Dx and earlier	6 years	1½ years
IC693CPU350-Ex , IC693CPU360-Ex, IC693CPU363-Ex and later	10 months	5½ months

PID Derivative Term

Optional filtering may now be applied to the PID Derivative Term to improve control loop stability in some applications. Filtering may be enabled by setting bit 5 (previously unused) in the Config Word parameter of the PID Parameter Block.

The following changes will be made to the *Series 90™-30/20/Micro PLC CPU Instruction Set Reference Manual*, GFK-0467M, at its next revision:

In Chapter 12, "Control Functions", Section "*PID Algorithm Selection (PIDISA or PIDIND) and Gains"*

The description of the Derivation term should be replaced with this text:

The Derivative term is the time rate of change of the Error term in the interval since the last PID solution.

Derivative = ΔError / dt = (Error – previous Error) / dt,

where

dt = Current PLC elapsed time - PLC elapsed time at previous PID solution.

In normal mode (that is, without Reverse-Action mode), this is the change in the error term.

(Error – previous Error) = (SP – PV) – (previous SP – previous PV)
= (previous PV – PV) – (previous SP – SP)

However, when the Error Polarity bit (bit 0) in the Config Word is set, the sign of the change in the error term is reversed.

(Error – previous Error) = (PV – SP) – (previous PV – previous SP)
= (PV – previous PV) – (SP – previous SP)

The change in the error term depends on changes in both the Set Point and the Process Variable. If the Set Point is constant, the difference between SP and the previous SP is zero and has no effect on the output. However, Set Point changes can cause large transient swings in the derivative term and hence the output. Loop stability may be improved by eliminating the effect of Set Point changes on the derivative term. Set the third bit (bit 2) of the Config Word to 1 to calculate the Derivative based only on the change in PV.

For bit 2 set in normal mode (bit 0 = 0),

(Error – previous Error) = (previous PV – PV),

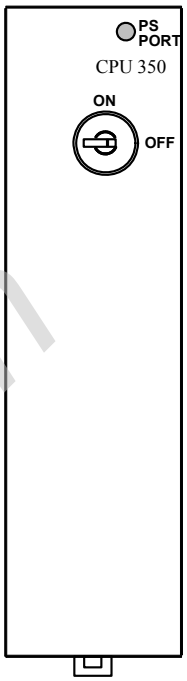
and with bit 2 set in Reverse-Action mode (bit 0 = 1),

(Error – previous Error) = (PV – previous PV).

In table 12-13 on page 12-82 of GFK-0467M, the Config Word row should be replaced with:

%Ref+0012	Config Word	Low 6 bits used	Bit 0: Error Polarity. When this bit is 0, the error term is SP - PV. When this bit is 1, the error term is PV - SP. Setting this bit to 1 modifies the standard PID Error Term from the normal (SP – PV) to (PV – SP), reversing the sign of the feedback term. This is for reverse acting controls where the CV must go down when the PV goes up. Bit 1: Output Polarity. When this bit is 0, the CV output represents the output of the PID calculation. When it is set to 1, the CV output represents the negative of output of the PID calculation. Setting this bit to 1 inverts the Output Polarity so that CV is the negative of the PID output rather than the normal positive value. Bit 2: When this bit is 1, the setpoint is removed from derivative calculation. For details, see the discussion on page 15. Bit 3: Deadband action. When the Deadband action bit is 0, no deadband action is chosen. If the error is within the deadband limits, the error is to be zero. Otherwise the error is not affected by the deadband limits. If the Deadband action bit is 1, deadband action is chosen. If the error is within the deadband limits, the error is forced to be zero. If, however, the error is outside the deadband limits, the error is reduced by the deadband limit (error = error – deadband limit). Bit 4: Anti-reset windup action. When this bit is 0, the anti-reset windup action uses a reset back calculation. When the output is clamped, this replaces the accumulated Y remainder value with whatever value is necessary to produce the clamped output exactly. When the bit is 1, this replaces accumulated Y term with the value of the Y term at the start of the calculation. In this way, the pre-clamp Y value is held as long as the output is clamped. Bit 5: Enable derivative filtering. When this bit is set to 0, no filtering is applied to the derivative term. **When set to 1, a first order filter is applied. This will limit the effects of higher frequency process disturbances on the derivative term.**

IC693CPU350 Specifications



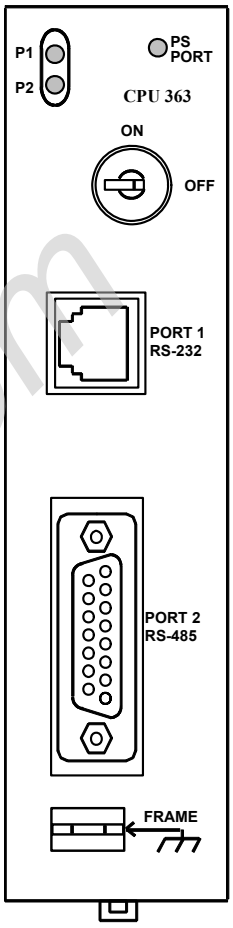
Total Baseplates per System	8 (CPU baseplate + 7 expansion and/or remote)
Load Required from Power Supply	670 milliamps from +5 VDC supply
Processor Speed	25 MegaHertz
Processor Type	80386EX
Typical Scan Rate	.22 milliseconds per 1K of logic (Boolean contacts)
User Program Memory (maximum)	48K Bytes (not configurable)
Discrete Input Points - %I	2,048
Discrete Output Points - %Q	2,048
Discrete Global Memory - %G	1,280 bits
Internal Coils - %M	4,096 bits
Output (Temporary) Coils - %T	256 bits
System Status References - %S	128 bits (%S, %SA, %SB, %SC - 32 bits each)
Register Memory - %R	9,999 words
Analog Inputs - %AI	2,048 words
Analog Outputs - %AQ	512 words
System Registers (for reference table viewing only; cannot be referenced in user logic program)	28 words (%SR)
Timers/Counters	>2,000
Shift Registers	Yes
Built-in Serial Port(s)	1 (uses connector on PLC power supply). Supports SNP, SNP-X slave protocols. Requires CMM module for SNP/SNP-X master, CCM, or RTU (slave) protocol support. Requires PCM module for RTU master support.
Communications	*LAN* – Supports multidrop. Also supports Ethernet, FIP, PROFIBUS, GBC, GCM, and GCM+ option modules.
Override	Yes
Battery Backed Clock	Yes
Interrupts	Supports the periodic subroutine feature.
Type of Memory Storage	RAM and Flash
PCM/CCM Compatibility	Yes
Floating Point Math Support	Yes, firmware-based in firmware releases 9.0 and later.

IC693CPU360 Specifications

Total Baseplates per System	8 (CPU baseplate + 7 expansion and/or remote)
Load Required from Power Supply	670 milliamps from +5 VDC supply
Processor Speed	25 MegaHertz
Processor Type	80386EX
Typical Scan Rate	0.22 milliseconds per 1K of logic (Boolean contacts)
User Program Memory (maximum)	240K (245,760) Bytes. Note: Actual size of available user program memory depends on the amounts configured for the %R, %AI, and %AQ configurable word memory types (described below).
Discrete Input Points - %I	2,048
Discrete Output Points - %Q	2,048
Discrete Global Memory - %G	1,280 bits
Internal Coils - %M	4,096 bits
Output (Temporary) Coils - %T	256 bits
System Status References - %S	128 bits (%S, %SA, %SB, %SC - 32 bits each)
Register Memory - %R	Configurable in 128 word increments, from 128 to 16,384 words with DOS programmer, and from 128 to 32,640 words with Windows programmer version 2.2 or VersaPro version 1.0.
Analog Inputs - %AI	Configurable in 128 word increments, from 128 to 8,192 words with DOS programmer, and from 128 to 32,640 words with Windows programmer version 2.2 or VersaPro version 1.0.
Analog Outputs - %AQ	Configurable in 128 word increments, from 128 to 8,192 words with DOS programmer, and from 128 to 32,640 words with Windows programmer version 2.2 or VersaPro version 1.0.
System Registers (for reference table viewing only; cannot be referenced in user logic program)	28 words (%SR)
Timers/Counters	>2,000
Shift Registers	Yes
Built-in Serial Port(s)	1 (uses connector on PLC power supply). Supports SNP, SNP-X slave protocols. Requires CMM module for SNP/SNP-X master, CCM, or RTU (slave) protocol support. Requires PCM module for RTU master support.
Communications	*LAN* – Supports multidrop. Also supports Ethernet, FIP, PROFIBUS, GBC, GCM, and GCM+ option modules.
Override	Yes
Battery Backed Clock	Yes
Interrupts	Supports the periodic subroutine feature.
Type of Memory Storage	RAM and Flash
PCM/CCM Compatibility	Yes
Floating Point Math Support	Yes, firmware-based in firmware release 9.0 and later.

IC693CPU363 Specifications

Total Baseplates per System	8 (CPU baseplate + 7 expansion and/or remote)
Load Required from Power Supply	890 milliamps from +5 VDC supply
Processor Speed	25 Megahertz
Processor Type	80386EX
Typical Scan Rate	.22 milliseconds per 1K of logic (Boolean contacts)
User Memory (total)	240K (245,760) Bytes. Note: Actual size of available user program memory depends on the amounts configured for the %R, %AI, and %AQ configurable word memory types (described below).
Discrete Input Points - %I	2,048
Discrete Output Points - %Q	2,048
Discrete Global Memory - %G	1,280 bits
Internal Coils - %M	4,096 bits
Output (Temporary) Coils - %T	256 bits
System Status References - %S	128 bits (%S, %SA, %SB, %SC - 32 bits each)
Register Memory - %R	Configurable in 128 word increments, from 128 to 16,384 words with DOS programmer, and from 128 to 32,640 words with Windows programmer version 2.2 or later, or VersaPro version 1.0 or later.
Analog Inputs - %AI	
Analog Outputs - %AQ	
System Registers (for reference table viewing only; cannot be referenced in user logic program)	28 words (%SR)
Timers/Counters	>2,000 (depends on available user memory)
Shift Registers	Yes
Built-in Serial Ports	3 (one uses connector on PLC power supply). Supports SNP/SNPX slave (on all three ports) and RTU slave and Serial I/O (on Ports 1 and 2). Requires CMM module for CCM and PCM module for RTU master.
Communications	*LAN* – Supports multidrop. Also supports Ethernet, FIP, PROFIBUS, GBC, GCM, and GCM+ option modules.
Override	Yes
Battery Backed Clock	Yes
Interrupt Support	Supports the periodic subroutine feature.
Type of Memory Storage	RAM and Flash
PCM/CCM Compatibility	Yes
Floating Point Math Support	Yes, firmware-based



Installation in Hazardous Locations

The following information is for products bearing the UL marking for Hazardous Locations:

- WARNING - EXPLOSION HAZARD - SUBSTITUTION OF COMPONENTS MAY IMPAIR SUITABILITY FOR CLASS I, DIVISION 2;
- WARNING - EXPLOSION HAZARD - WHEN IN HAZARDOUS LOCATIONS, TURN OFF POWER BEFORE REPLACING OR WIRING MODULES; AND
- WARNING - EXPLOSION HAZARD - DO NOT CONNECT OR DISCONNECT EQUIPMENT UNLESS POWER HAS BEEN SWITCHED OFF OR THE AREA IS KNOWN TO BE NONHAZARDOUS.
- EQUIPMENT LABELED WITH REFERENCE TO CLASS I, GROUPS A, B, C & D, DIV. 2 HAZARDOUS LOCATIONS IS SUITABLE FOR USE IN CLASS I, DIVISION 2, GROUPS A, B, C, D OR NON-HAZARDOUS LOCATIONS ONLY.