MITSUBISHI

PROGRAMMABLE CONTROLLER

MELSEC-A

User's Manual

Interruption input module type A1SI61 (Hardware)

INTRODUCTION

Thank you for choosing the Mitsubishi MELSEC-A Series of General Purpose Programmable Controllers Please read this manual carefully so that the equipment is used to its optimum A copy of this manual should be forwarded to the end User

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Specifications subject to change without notice

1. GENERAL DESCRIPTION

1 GENERAL DESCRIPTION

This User's Manual explains the specifications, the handling methods and how to use an A1SI61 type interrupt module (hereafter called the A1SI61) that is utilized with an AnSCPU.

An A1SI61 has an interrupt function to interrupt processing of main sequence program, and then, executes the designated interrupt program when an interrupt input is given

(1) An A1SI61 is applicable to the AnSCPU

(2) Only one A1SI61 can be installed in an AnSCPU system

REMARK

The ACPU Programming Manual (Fundamentals) gives details of interrupt programs

2. SPECIFICATIONS

2 SPECIFICATIONS

2.1 General Specifications

Item	Specifications				
Operating ambient temperature	0 to 55 °C (See the important notice described below)				
Storage ambient temperature	–20 to 75 °C				
Operating ambient humidity	10 to 90% RH, non condensing				
Storage ambient humidity	10 to 90% RH, non condensing				
Vibration resistance	Conforms to *2JIS C 0911	Frequency	Acceleration	Amplitude	Sweep Count
		10 to 55 Hz	—	0 075 mm (0 003 in)	10 times *1 (1 octave/ minute)
		55 to 150 Hz	9 8 m/s^2 (1g)	—	
Shock resistance	Conforms to *2JIS C 0912 (98 m/s^2 (10g) x 3 times in 3 directions)				
Noise durability	By noise simulator of 1500 Vpp voltage,1 µsec noise width and 25 to 60 Hz noise frequency				
Dielectric withstand voltage	1500 VAC for 1 minute across AC external terminals and ground 500 VAC for 1 minute across DC external terminals and ground				
Insulation resistance	5 MΩ or greater by 500 VDC insulation resistance tester across AC external terminals and ground				
Grounding	Class 3 grounding; Ground to the panel if proper grounding is not available				
Operating ambience	Free of corrosive gases Dust should be minimal				
Cooling method	Self-cooling				

REMARKS

(1) One octave marked *1 indicates a change from the initial frequency to double or half frequency For example, any of the changes from 10 to 20 Hz, from 20 to 40 Hz, or 20 to 10 Hz are referred to as one octave

(2) *2JIS Japanese Industrial Standard

IMPORTANT

Restriction for UL standard approved products

In order to be recognized as UL listed products, the following restructions apply:

(1) Operating ambient temperature is limited from 0 to 50°C

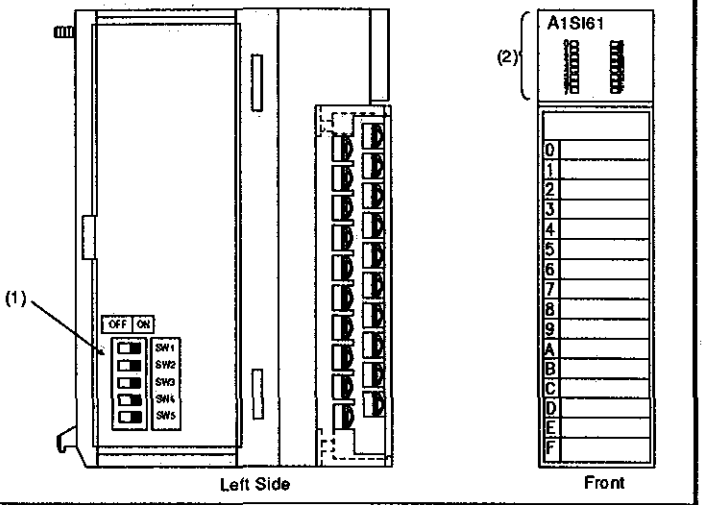
(2) A class 2 power supply recognized by the UL standard must be used

2 2 Performance Specifications

Items		Specifications	
Number of interrupt points		16 points (interrupt processing condition setting is in 4 point units)	
Number of occupied I/O points		32 points	
Isolation method		Photocoupler insulation	
Rated input voltages		12 VDC	24 VDC
Rated input currents		Approx 4 mA	Approx 8 mA
Operating voltage range		10 2 to 26 4 VDC	
Max number of simultaneous input		100 % simultaneous ON	
ON voltage/ON current		9 V or more/3 mA or more	
OFF voltage/OFF current		4 V or less/1 mA or less	
Input resistance		Approx 2 7 kΩ	
Response time	OFF → ON	0 2 msec or less	
	ON → OFF	0 2 msec or less	
Internal current consumption (5 VDC)		57 mA (TYP, all points ON)	
Common method		16 points/common	
Operation display		ON display (LED)	
External connection method		20 points terminal block connectors (M3 5 x 7 screws)	
Applicable wire gauges		0 75 to 1 5 mm^2	
Applicable solderless terminals		1 25 3, 1 25-YS3A V1 25 3 V1 25-YS3A	
Weight kg (lb)		0 2 (0 44)	

3. NOMENCLATURE

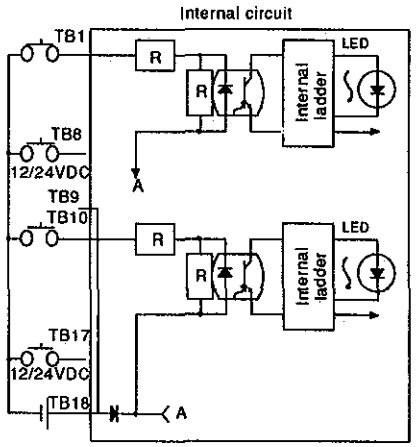
3. Nomenclature



No	Name & Contents			
(1)	Interrupt mode switch			
	Either of leading edge (RISE) or trailing edge (FALL) of input signal can be selected as timing to generate an interrupt signal to a PC CPU Can be selected in 4-point unit. Factory-set = ON			
	Switch	**Terminal Number**	**OFF**	**ON**
	SW1	0 to 3	FALL	RISE
	SW2	4 to 7		
	SW3	8 to B		
	SW4	C to F		
	SW5	Unused	NC	
(2)	Input display LED Displays the input ON/OFF state Lit when ON			

4. EXTERNAL CONNECTIONS

4 EXTERNAL CONNECTIONS



External Connections	Terminal No	Signal Name
	TB1	X00
	TB2	X01
	TB3	X02
	TB4	X03
	TB5	X04
	TB6	X05
	TB7	X06
	TB8	X07
	TB9	COM
	TB10	X08
	TB11	X09
	TB12	X0A
	TB13	X0B
	TB14	X0C
	TB15	X0D
	TB16	X0E
	TB17	X0F
	TB18	COM
	TB19	Vacant
	TB20	Vacant

POINTS

(1) User cannot use Y00 to Y0F

(2) Keep signal wires as far away as possible from power lines or main circuit cables

5. INTERRUPT PROCESSING

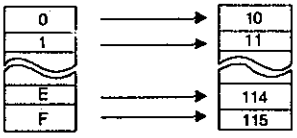
5 INTERRUPT PROCESSING

5 1 Designating an Interrupt Program (I0 to I15)

The A1SI61 can activate 16 interrupt programs (I0 to I15) which correspond to interrupt inputs 0 to F

When an interrupt signal is given to terminal number 0 and a slide switch is set to RISE, the processing jumps to interrupt pointer I0 and the interrupt program is executed

Interrupt pointer numbers (I) which correspond to A1SI61 terminal numbers is given below



A1SI61 terminal numbers Interrupt pointers (program)

POINT

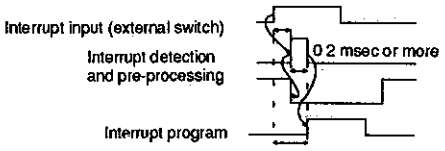
Besides interrupt from an A1SI61, I16 to I23 (Special function module interrupts) and I29 to I31 (real time interrupts) are also available
Priorities of the interrupts are as follows;
(High) I16 to I23 – I0 to I16 – I31 – I30 – I29 (Low)

5.2 Interrupt Signal Pulse Width

The response time of an A1SI61 is 0 2 msec from OFF to ON

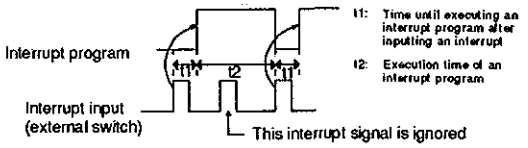
Therefore, pulse width of an interrupt signal is 0 2 msec or longer

If the pulse width is less than 0 2 msec, the interrupt may not be received



5.3 Minimum Interval When Repeating the Same Interrupt Continuously

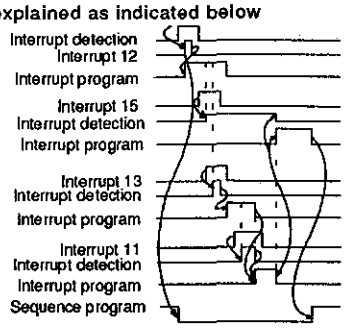
Time between same interrupt signals should be greater than sum of time from a signal given to the module to an interrupt program activated and time necessary to process the interrupt program
If a interrupt signal is given while the same interrupt is still in process, the interrupt given later could be ignored



5 4 Interrupt Processing Priorities

If several interrupt factors occur during interrupt processing, the youngest input number has the highest priority

This is explained as indicated below



In this example, the order of execution is

I2 → I3 → I1 → I5

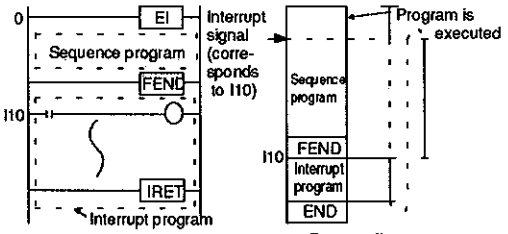
Even if an interrupt factor occurs in the order of I5 and I3 during processing of interrupt I2, the interrupt program of I3 whose interrupt number (pointer) is younger has priority over I5 Therefore, after processing I2, I3 is executed

And, during executing of the I3 interrupt program, the I1 interrupt factor occurs Therefore, after processing of I3, the interrupt program of I1 will be executed Then I5 will be executed

5 5 Creating an Interrupt Program

Create an interrupt program after a sequence program (after the FEND instruction and before the END instruction) Enter the interrupt pointer I[ ][ ] at the head (the left side of a bus) of an interrupt program

And then, enter an IRET instruction at the end of the interrupt program



Sample of interrupt program ladder Program flow

POINTS

(1) Unless an EI instruction is executed to be the EI state, interrupt programs are not activated

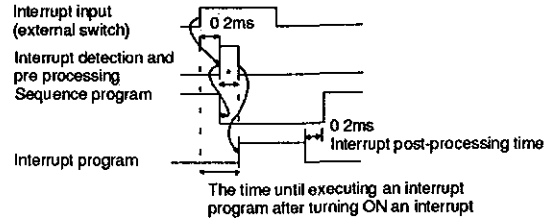
(2) Interrupt signals given during the DI state activate their corresponding interrupt programs after an EI instruction is executed

(3) Interrupt signals given during STOP of PC CPU activate their corresponding interrupt programs after the PC CPU is turned to RUN and an EI instruction is executed

6. INTERRUPT PROCESSING TIMING

6 Interrupt Processing Timing

The time to actually execute an interrupt program is delayed even when an interrupt signal is input In addition, execution of a program will be delayed if an interrupt is input while executing other interrupts as explained below



Time length marked * depends on in which processing of a CPU the signal is given If an interrupt signal given while move than one of processings listed in the table is being executed, time length marked * will be sum of the delay times of each processing

There is some delay time from interrupt signal input to activation of its interrupt program In addition, there is additional delay time if an interrupt signal is given during processing of another interrupt

The values are as follows (The following shows maximum values)

Item	A Sequence is being Executed Normally	A Program from I29 to I31 is being Executed.	Communications with an A1SJ71C24 and AD51, etc	Data Link Interrupt is being Processed	Monitor Interrupt is being Processed, Peripheral Device Interrupt
Value of *	0 2 msec	1 msec + execution time of the interrupt program of I29 to I31	1 5 msec	0 5 msec	0 65 msec (In case of monitoring it the device of 128 bytes)

The time of * when the processing overlaps on the previous page is the total time of the individual value

[Sample calculation]

If an interrupt is executed from an A1SI61 during communication with A1SJ71C24

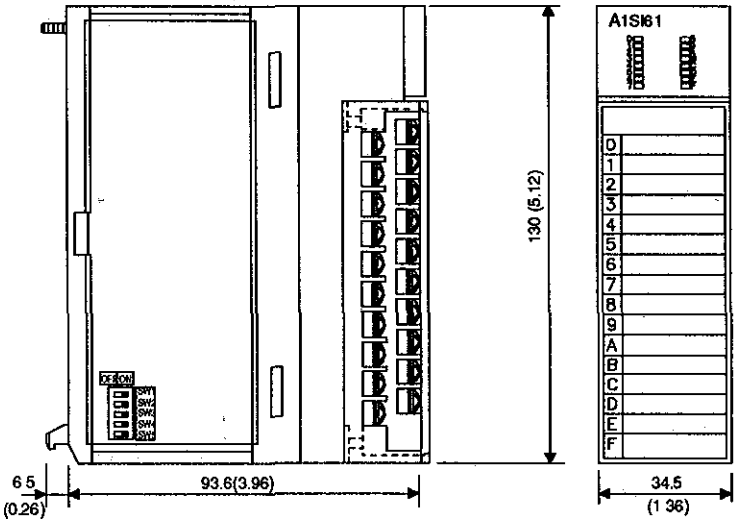
* Value = 0 2 + 1 5 msec

POINT

Even if a basic instruction and an application instruction are being executed, they are interrupted and an interrupt program is executed according to the timing indicated above

7. OUTSIDE DIMENSIONS

7 OUTSIDE DIMENSIONS



Unit mm(inch)

REVISIONS

A Apr., 1994	

IMPORTANT

(1) Design the configuration of a system to provide an external protective or safety interlocking circuit for the CPs

(2) The components on the printed circuit boards will be damaged by static electricity, so avoid handling them directly If it is necessary to handle them take the following precautions

(a) Ground human body and work bench

(b) Do not touch the conductive areas of the printed circuit board and its electrical parts with and non-grounded tools etc